
HM624100H Series

4M High Speed SRAM (1-Mword × 4-bit)

HITACHI

ADE-203-789D (Z)
Rev. 1.0
Sep. 15, 1998

Description

The HM624100H is a 4-Mbit high speed static RAM organized 1-Mword × 4-bit. It has realized high speed access time by employing CMOS process (4-transistor + 2-poly resistor memory cell) and high speed circuit designing technology. It is most appropriate for the application which requires high speed and high density memory, such as cache and buffer memory in system. The HM624100H is packaged in 400-mil 32-pin SOJ for high density surface mounting.

Features

- Single 5.0 V supply : 5.0 V ± 10 %
- Access time 10/12/15 ns (max)
- Completely static memory
 - No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible
 - All inputs and outputs
- Operating current : 200/180/160 mA (max)
- TTL standby current : 70/60/50 mA (max)
- CMOS standby current : 5 mA (max)
 - : 1.2 mA (max) (L-version)
- Data retention current : 0.8 mA (max) (L-version)
- Data retention voltage : 2.0 V (min) (L-version)
- Center V_{CC} and V_{SS} type pinout

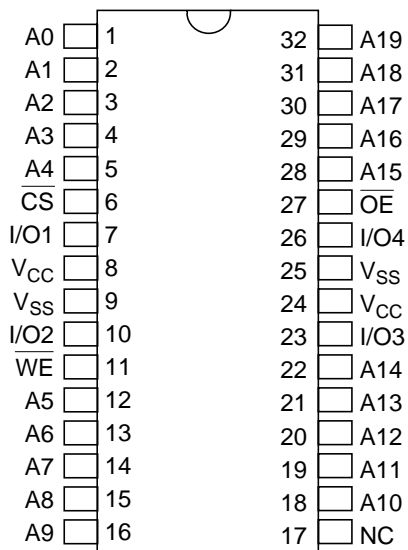
HM624100H Series

Ordering Information

Type No.	Access time	Package
HM624100HJP-10	10 ns	400-mil 32-pin plastic SOJ (CP-32DB)
HM624100HJP-12	12 ns	
HM624100HJP-15	15 ns	
HM624100HLJP-10	10 ns	
HM624100HLJP-12	12 ns	
HM624100HLJP-15	15 ns	

Pin Arrangement

HM624100HJP/HLJP Series

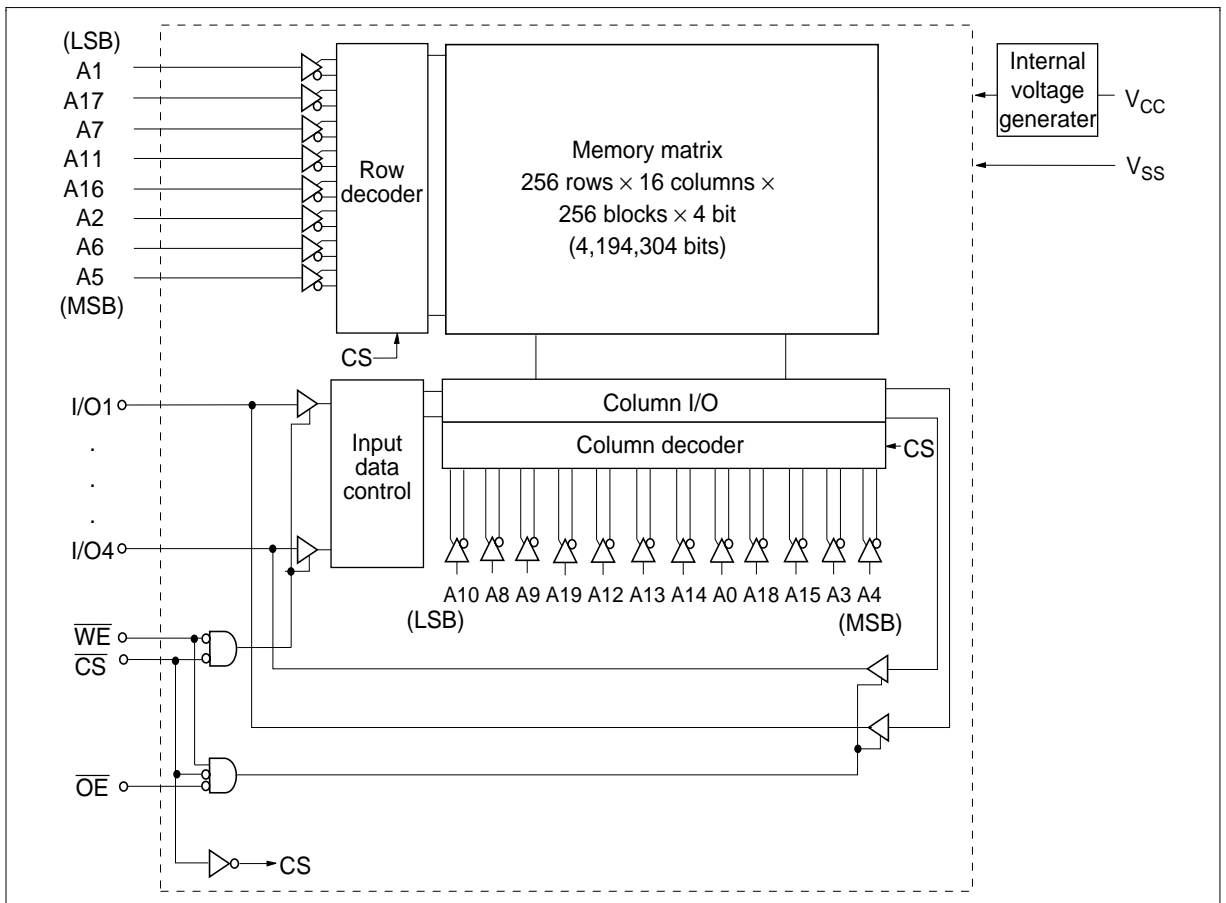


(Top view)

Pin Description

Pin name	Function
A0 to A19	Address input
I/O1 to I/O4	Data input/output
CS	Chip select
OE	Output enable
WE	Write enable
V _{CC}	Power supply
V _{SS}	Ground
NC	No connection

Block Diagram



Operation Table

CS	OE	WE	Mode	V _{CC} current	I/O	Ref. cycle
H	×	×	Standby	I _{SB} , I _{SB1}	High-Z	—
L	H	H	Output disable	I _{CC}	High-Z	—
L	L	H	Read	I _{CC}	Dout	Read cycle (1) to (3)
L	H	L	Write	I _{CC}	Din	Write cycle (1)
L	L	L	Write	I _{CC}	Din	Write cycle (2)

Note: ×: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V _{SS}	V _{CC}	-0.5 to +7.0	V
Voltage on any pin relative to V _{SS}	V _T	-0.5* ¹ to V _{CC} +0.5* ²	V
Power dissipation	P _T	1.0	W
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +125	°C
Storage temperature under bias	T _{bias}	-10 to +85	°C

- Notes: 1. V_T (min) = -2.0 V for pulse width (under shoot) ≤ 8 ns
 2. V_T (max) = V_{CC} + 2.0 V for pulse width (over shoot) ≤ 8 ns

Recommended DC Operating Conditions (T_a = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC} * ³	4.5	5.0	5.5	V
	V _{SS} * ⁴	0	0	0	V
Input voltage	V _{IH}	2.2	—	V _{CC} + 0.5* ²	V
	V _{IL}	-0.5* ¹	—	0.8	V

- Notes: 1. V_{IL} (min) = -2.0 V for pulse width (under shoot) ≤ 8 ns
 2. V_{IH} (max) = V_{CC} + 2.0 V for pulse width (over shoot) ≤ 8 ns
 3. The supply voltage with all V_{CC} pins must be on the same level.
 4. The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0\text{V}$)

Parameter		Symbol	Min	Typ* ¹	Max	Unit	Test conditions
Input leakage current		I_{L1}	—	—	2	μA	$V_{in} = V_{SS}$ to V_{CC}
Output leakage current		I_{LO}	—	—	2	μA	$V_{in} = V_{SS}$ to V_{CC}
Operation power supply current	10 ns cycle	I_{CC}	—	—	200	mA	Min cycle $\overline{CS} = V_{IL}$, $I_{out} = 0\text{ mA}$ Other inputs = V_{IH}/V_{IL}
	12 ns cycle	I_{CC}	—	—	180		
	15 ns cycle	I_{CC}	—	—	160		
Standby power supply current	10 ns cycle	I_{SB}	—	—	70	mA	Min cycle, $\overline{CS} = V_{IH}$, Other inputs = V_{IH}/V_{IL}
	12 ns cycle	I_{SB}	—	—	60		
	15 ns cycle	I_{SB}	—	—	50		
		I_{SB1}	—	0.1	5	mA	$f = 0\text{ MHz}$ $V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2\text{ V}$, (1) $0\text{ V} \leq V_{in} \leq 0.2\text{ V}$ or (2) $V_{CC} \geq V_{in} \geq V_{CC} - 0.2\text{ V}$
			—* ²	0.1* ²	1.2* ²		
Output voltage		V_{OL}	—	—	0.4	V	$I_{OL} = 8\text{ mA}$
		V_{OH}	2.4	—	—	V	$I_{OH} = -4\text{ mA}$

Notes: 1. Typical values are at $V_{CC} = 5.0\text{ V}$, $T_a = +25^\circ\text{C}$ and not guaranteed.

2. This characteristics is guaranteed only for L-version.

Capacitance ($T_a = +25^\circ\text{C}$, $f = 1.0\text{ MHz}$)

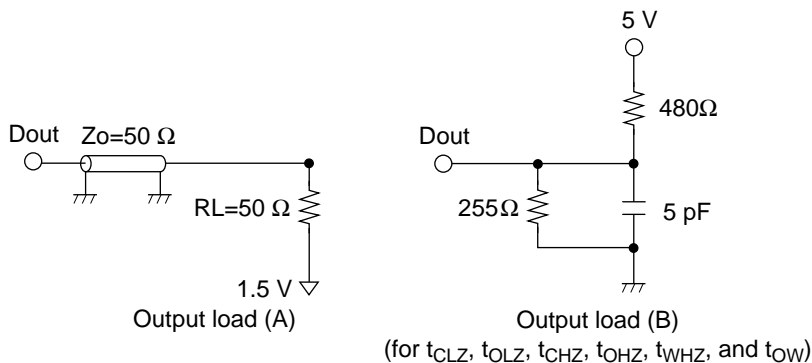
Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance* ¹		C_{in}	—	—	6	pF	$V_{in} = 0\text{ V}$
Input/output capacitance* ¹		$C_{i/O}$	—	—	8	pF	$V_{i/O} = 0\text{ V}$

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, unless otherwise noted.)

Test Conditions

- Input pulse levels: 3.0 V/0.0 V
- Input rise and fall time: 3 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures (Including scope and jig)



Read Cycle

Parameter	Symbol	HM624100H						Unit	Notes
		-10		-12		-15			
		Min	Max	Min	Max	Min	Max		
Read cycle time	t_{RC}	10	—	12	—	15	—	ns	
Address access time	t_{AA}	—	10	—	12	—	15	ns	
Chip select access time	t_{ACS}	—	10	—	12	—	15	ns	
Output enable to output valid	t_{OE}	—	5	—	6	—	7	ns	
Output hold from address change	t_{OH}	3	—	3	—	3	—	ns	
Chip select to output in low-Z	t_{CLZ}	3	—	3	—	3	—	ns	1
Output enable to output in low-Z	t_{OLZ}	0	—	0	—	0	—	ns	1
Chip deselect to output in high-Z	t_{CHZ}	—	5	—	6	—	7	ns	1
Output disable to output in high-Z	t_{OHZ}	—	5	—	6	—	7	ns	1

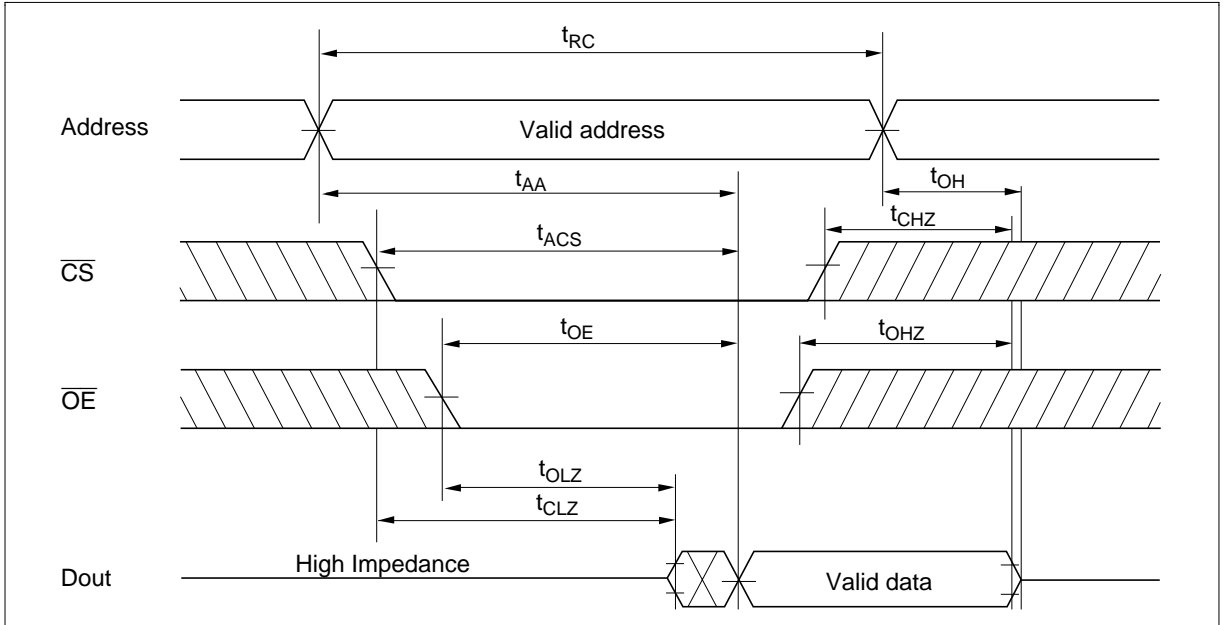
Write Cycle

Parameter	Symbol	HM624100H						Unit	Notes
		-10		-12		-15			
		Min	Max	Min	Max	Min	Max		
Write cycle time	t_{WC}	10	—	12	—	15	—	ns	
Address valid to end of write	t_{AW}	7	—	8	—	10	—	ns	
Chip select to end of write	t_{CW}	7	—	8	—	10	—	ns	9
Write pulse width	t_{WP}	7	—	8	—	10	—	ns	8
Address setup time	t_{AS}	0	—	0	—	0	—	ns	6
Write recovery time	t_{WR}	0	—	0	—	0	—	ns	7
Data to write time overlap	t_{DW}	5	—	6	—	7	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns	
Write disable to output in low-Z	t_{OW}	3	—	3	—	3	—	ns	1
Output disable to output in high-Z	t_{OHZ}	—	5	—	6	—	7	ns	1
Write enable to output in high-Z	t_{WHZ}	—	5	—	6	—	7	ns	1

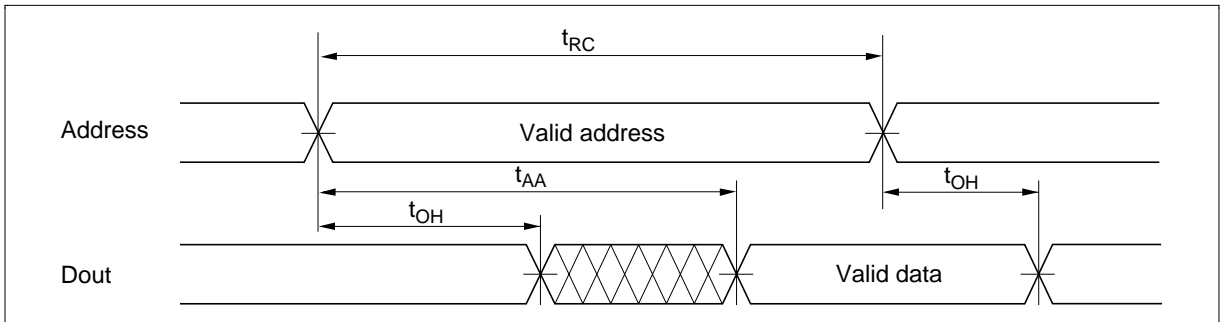
- Note:
1. Transition is measured ± 200 mV from steady voltage with Load (B). This parameter is sampled and not 100% tested.
 2. Address should be valid prior to or coincident with \overline{CS} transition low.
 3. \overline{WE} and/or \overline{CS} must be high during address transition time.
 4. If \overline{CS} and \overline{OE} are low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
 5. If the \overline{CS} low transition occurs simultaneously with the \overline{WE} low transition or after the \overline{WE} transition, output remains a high impedance state.
 6. t_{AS} is measured from the latest address transition to the later of \overline{CS} or \overline{WE} going low.
 7. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going high to the first address transition.
 8. A write occurs during the overlap of a low \overline{CS} and a low \overline{WE} . A write begins at the latest transition among \overline{CS} going low and \overline{WE} going low. A write ends at the earliest transition among \overline{CS} going high and \overline{WE} going high. t_{WP} is measured from the beginning of write to the end of write.
 9. t_{CW} is measured from the later of \overline{CS} going low to the the end of write.

Timing Waveforms

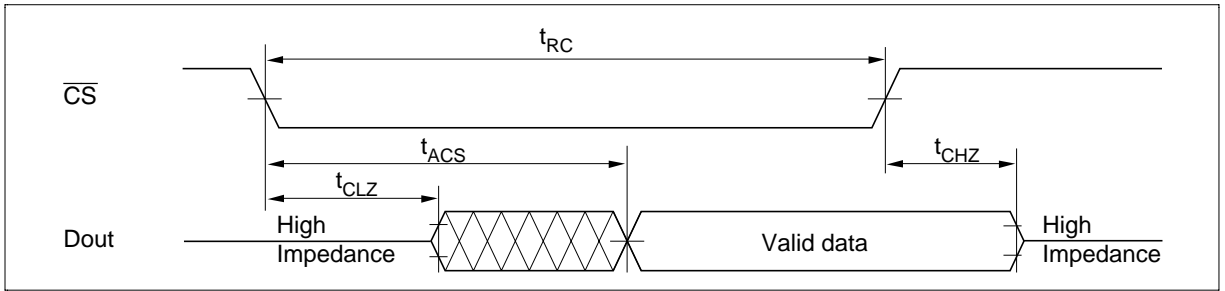
Read Timing Waveform (1) ($\overline{WE} = V_{IH}$)



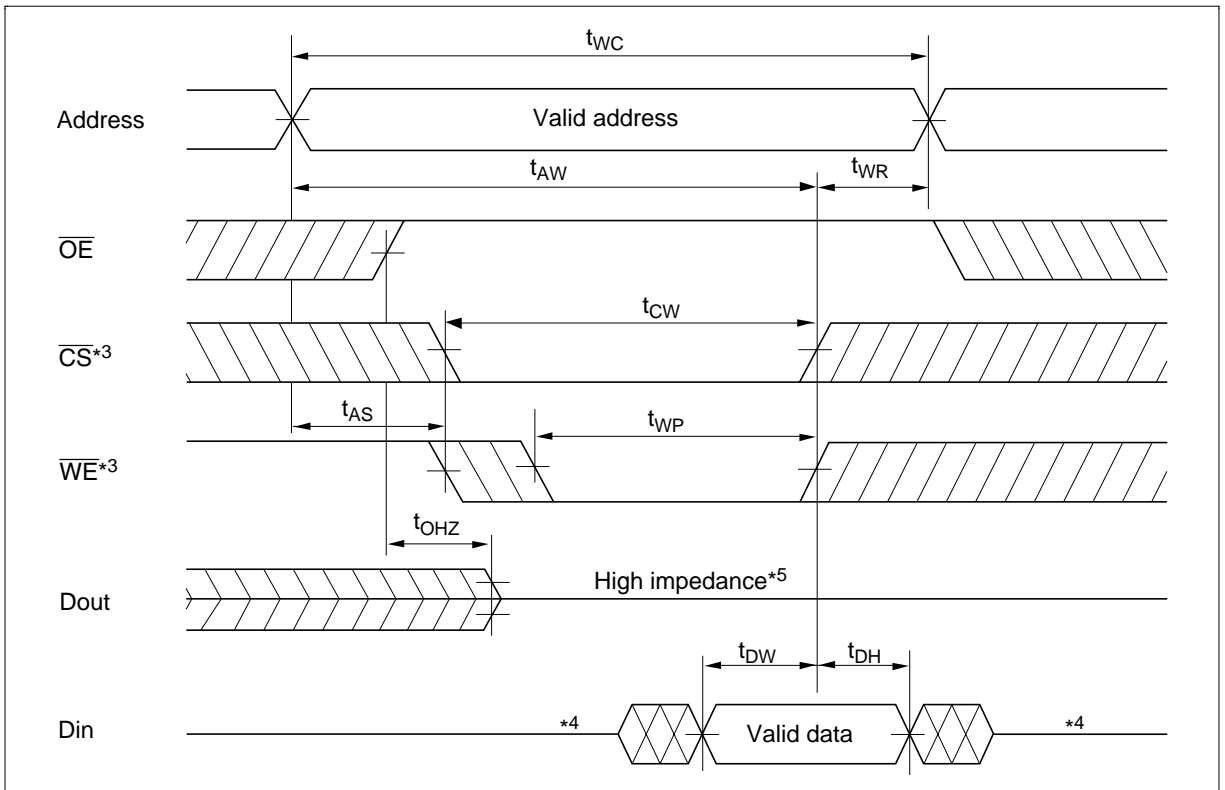
Read Timing Waveform (2) ($\overline{WE} = V_{IH}$, $\overline{CS} = V_{IL}$, $\overline{OE} = V_{IL}$)



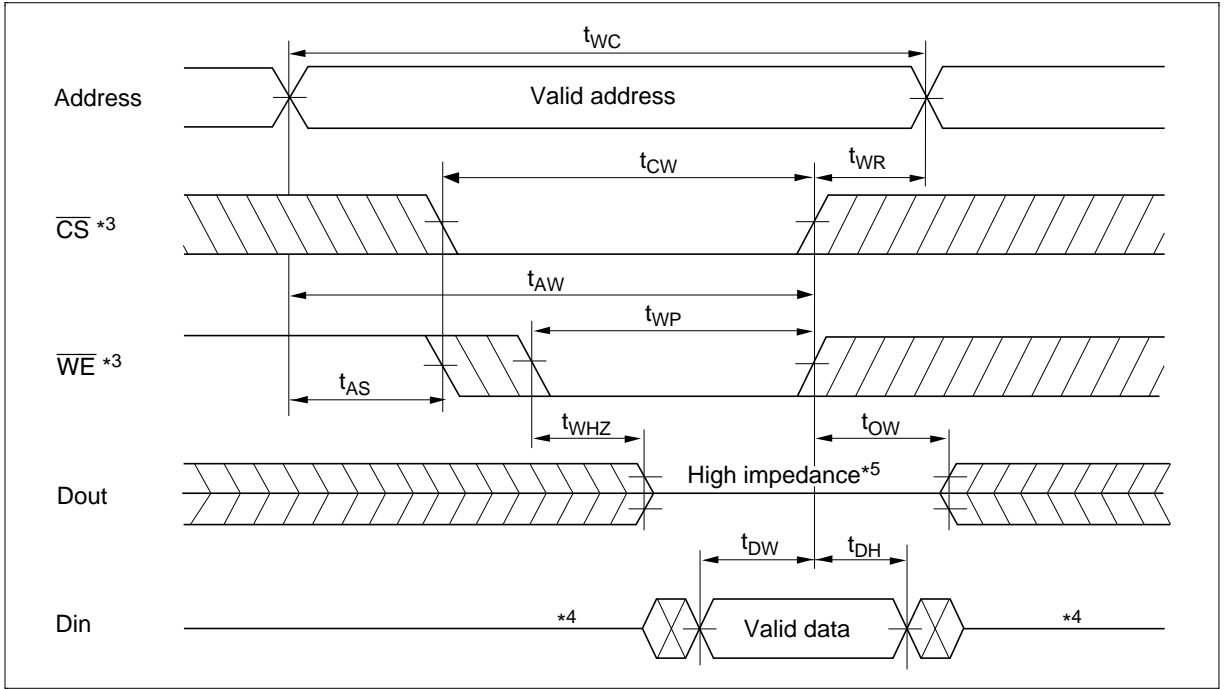
Read Timing Waveform (3) ($\overline{WE} = V_{IH}, \overline{CS} = V_{IL}, \overline{OE} = V_{IL}$)*2



Write Timing Waveform (1) (\overline{WE} Controlled)



Write Timing Waveform (2) (\overline{CS} Controlled)



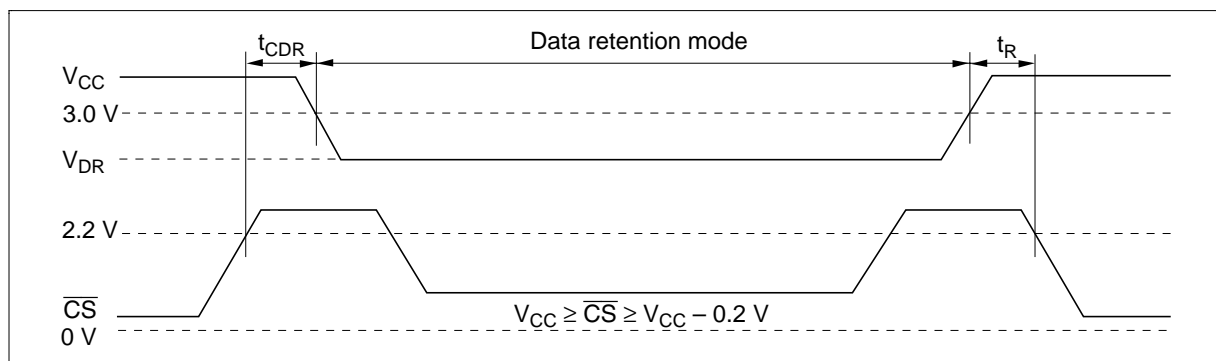
Low V_{CC} Data Retention Characteristics ($T_a = 0$ to $+70^\circ\text{C}$)

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2$ V (1) 0 V \leq $V_{in} \leq 0.2$ V or (2) $V_{CC} \geq V_{in} \geq V_{CC} - 0.2$ V
Data retention current	I_{CCDR}	—	50	800	μA	$V_{CC} = 3$ V, $V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2$ V (1) 0 V \leq $V_{in} \leq 0.2$ V or (2) $V_{CC} \geq V_{in} \geq V_{CC} - 0.2$ V
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	5	—	—	ms	

Note: 1. Typical values are at $V_{CC} = 3.0$ V, $T_a = +25^\circ\text{C}$, and not guaranteed.

Low V_{CC} Data Retention Timing Waveform

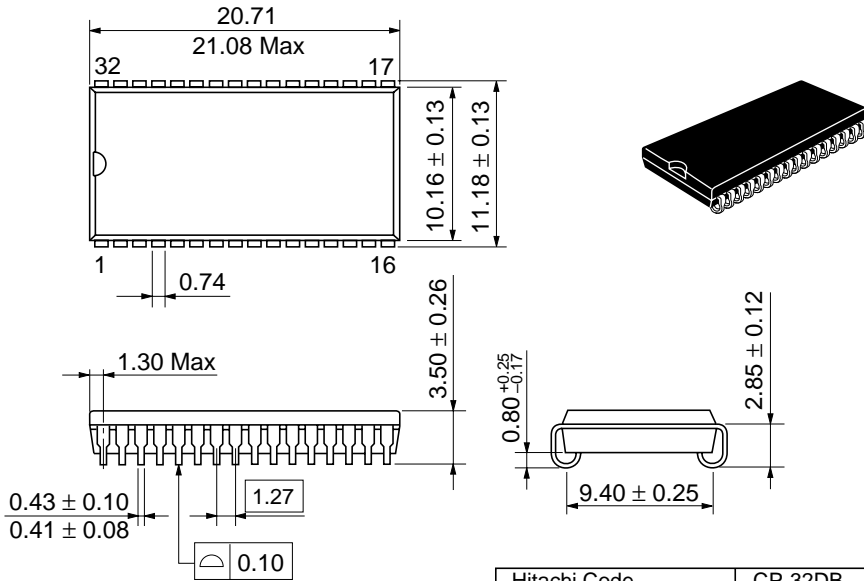


HM624100H Series

Package Dimensions

HM624100HJP/HLJP Series (CP-32DB)

Unit: mm



Dimension including the plating thickness
Base material dimension

Hitachi Code	CP-32DB
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.2 g

Cautions

1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.
2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.
3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.
4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.
5. This product is not designed to be radiation resistant.
6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.
7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.

HITACHI

Hitachi, Ltd.

Semiconductor & IC Div.
 Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
 Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL NorthAmerica : <http://semiconductor.hitachi.com/>
 Europe : <http://www.hitachi-eu.com/hel/ecg>
 Asia (Singapore) : <http://www.has.hitachi.com.sg/grp3/sicd/index.htm>
 Asia (Taiwan) : http://www.hitachi.com.tw/E/Product/SICD_Frame.htm
 Asia (HongKong) : <http://www.hitachi.com.hk/eng/bo/grp3/index.htm>
 Japan : <http://www.hitachi.co.jp/Sicd/indx.htm>

For further information write to:

Hitachi Semiconductor
 (America) Inc.
 2000 Sierra Point Parkway
 Brisbane, CA 94005-1897
 Tel: <1> (800) 285-1601
 Fax: <1> (303) 297-0447

Hitachi Europe GmbH
 Electronic components Group
 Dornacher Straße 3
 D-85622 Feldkirchen, Munich
 Germany
 Tel: <49> (89) 9 9180-0
 Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
 Electronic Components Group.
 Whitebrook Park
 Lower Cookham Road
 Maidenhead
 Berkshire SL6 8YA, United Kingdom
 Tel: <44> (1628) 585000
 Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
 16 Collyer Quay #20-00
 Hitachi Tower
 Singapore 049318
 Tel: 535-2100
 Fax: 535-1533

Hitachi Asia Ltd.
 Taipei Branch Office
 3F, Hung Kuo Building, No.167,
 Tun-Hwa North Road, Taipei (105)
 Tel: <886> (2) 2718-3666
 Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
 Group III (Electronic Components)
 7/F., North Tower, World Finance Centre,
 Harbour City, Canton Road, Tsim Sha Tsui,
 Kowloon, Hong Kong
 Tel: <852> (2) 735 9218
 Fax: <852> (2) 730 0281
 Telex: 40815 HITEC HX

Copyright © Hitachi, Ltd., 1998. All rights reserved. Printed in Japan.